REMARKS/ARGUMENT

Prior to discussing the merits of the rejection, Applicant notes that there seems to be an error in the rejection on page 2 of the Office Action dated July 27, 2006. Paragraph 2 identifies the rejection as: Claims 1-9 and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Gorman et al., US PG Pub 2004/0218454. However, Examiner's arguments address only Claims 1-9 and 11-22 under 35 U.S.C. 102(e) as being anticipated by Gorman et al., US PG Pub 2004/0218454. Claim 10 is subsequently rejected under 35 U.S.C. 103(a). Applicant's arguments below assume that Claim 10 was not rejected under 35 U.S.C. 102(e).

1) Claims 1-9 and 11-22 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gorman et al., US PG Pub 2004/0218454. Applicant respectfully traverses this rejection as set forth below.

In order that the rejection of Claims 1-9 and 11-22 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, an electronic device, comprising: "a memory structure comprising an integer *M* of memory word slots, wherein each memory word slot is operable to store an integer *N* of bits", "a scan storage circuit, operable to receive a scan word having a number of bits less than *MxN*" and "control circuitry for causing successive scan words to be written into the scan storage circuit, for causing successive scan words to be **written from the scan storage circuit into all of the memory word slots of the memory structure**, and for causing successive scan words to be **read from all of the memory word slots of the memory structure into the scan storage circuit**".

Independent Claim 18, as amended, requires and positively recites, a method of operating an electronic device, the device comprising "a memory structure comprising an integer *M* of memory word slots, wherein each memory word slot is operable to store an integer *N* of bits", "causing successive scan words to be written into a scan storage circuit, the scan storage circuit operable to receive a scan word having a number of bits less than *MxN*", "causing successive scan words to be **written from the scan storage circuit into all of the memory word slots of the memory structure**" and "causing successive scan words to be **read from all of the memory word slots of the memory structure into the scan storage circuit**".

In contrast, Gorman discloses an apparatus discloses "a structure and method for serially retrieving fuse information to and from a non-scannable static random access memory (SRAM) array within an embedded DRAM structure" (paragraph [0006], lines 1-4). Gorman goes on to disclose that the "fuse information comprises a listing of activated fuses (those fuses that have been blown in order to replace defective devices with properly operating devices within the DRAM array)(paragraph [0007], lines 1-4). As such, Gorman fails to teach or suggest, "control circuitry for causing successive scan

words to be written into the scan storage circuit, for causing successive scan words to be **written from the scan storage circuit into all of the memory word slots of the memory structure**, and for causing successive scan words to be **read from all of the memory word slots of the memory structure into the scan storage circuit**", as required by Claim 1, as amended, OR "causing successive scan words to be **written from the scan storage circuit into all of the memory word slots of the memory structure**" and "causing successive scan words to be **read from all of the memory word slots of the memory structure into the scan storage circuit**", as required by Claim 18, as amended. Accordingly, the 35 U.S.C. 102(e) rejection of Claims 1 and 18 is improper and must be withdrawn since "each and every element as set forth in the claim CANNOT be found, either expressly or inherently described, in a single prior art reference", as required by law.

Claims 2-9, 11-17 and 19-22 stand allowable as depending directly, or indirectly, from respective allowable Claim 1.

Claim 2 further defines the electronic device of claim 1 wherein the scan storage circuit is operable to receive a scan word consisting of *N* bits. Claim 2 stands allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 3 further defines the electronic device of claim 2 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit. Claim 3 stands allowable for the same reasons set forth above in support of the allowance of Claim 2.

Claim 4 further defines the electronic device of claim 3 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit. Claim 4 stands allowable for the same reasons set forth above in support of the allowance of Claim 3.

Claim 5 further defines the electronic device of claim 4 wherein the scan storage circuit further comprises circuitry for causing each successive scan word **to be written from the scan storage circuit into the memory structure in parallel**, and for causing each successive scan word **to be read from the memory structure into the scan storage circuit in parallel**. Claim 5 stands allowable for the same reasons set forth above in support of the allowance of Claim 4. Moreover, Gorman specifically states the following:

> The shift register is utilized to collect the data that is received serially and then load multiple bits in parallel to the SRAM (because data is preferably written to the SRAM array in parallel operations and **not serially**)(paragraph [0007], lines 4-8).

Accordingly, Gorman fails to teach or suggest, "...circuitry for causing each successive scan word **to be written from the scan storage circuit into the memory structure in parallel**, and for causing each successive scan word **to be read from the memory structure into the scan storage circuit in parallel**", as further required by Claim 5.

Claim 6 further defines the electronic device of claim 5: "wherein the successive scan words to be written into the scan storage circuit **comprise a test sequence**" and "further comprising circuitry for comparing the successive scan words to be read from the memory structure **to the test sequence**". Claim 6 stands allowable for the same reasons set forth above in support of the allowance of Claim 5. Moreover, since Gorman specifically discloses "a structure and method for serially retrieving fuse information to and from a non-scannable static random access memory (SRAM) array within an embedded DRAM structure" (paragraph [0006], lines 1-4), and goes on to disclose that the "fuse information comprises a listing of activated fuses (those fuses that have been blown in order to replace defective devices with properly operating devices within the DRAM array)(paragraph [0007], lines 1-4), Gorman fails to teach or suggest, "wherein the successive scan words to be written into the scan storage circuit **comprise a test sequence**" and "further comprising circuitry for comparing the successive scan words to be read from the memory structure **to the test sequence**", as further required by Claim 6.

Claim 7 further defines the electronic device of claim 6: "wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells" and "wherein each set of N memory cells comprises N latches". Claim 7 stands allowable for the same reasons set forth above in support of the allowance of Claim 6.

Claim 8 further defines the electronic device of claim 7 wherein each of the *N* latches comprises: "a first inverter having an input providing an input to the latch and an output providing an output of the latch" and "a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch". Claim 8 stands allowable for the same reasons set forth above in support of the allowance of Claim 7.

Claim 9 further defines the electronic device of claim 7 wherein each memory word slot is operable to store the integer *N* of bits in a corresponding set of *N* memory cells and wherein each set of *N* memory cells is operable to store incoming data without responding to a clock transition. Claim 9 stands allowable for the same reasons set forth above in support of the allowance of Claim 7. Further, there is no teaching or suggestion in Gorman that its "...memory cells are operable to store incoming data without responding to a clock transition".

Claim 11 further defines the electronic device of claim 1 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit. Claim 11 stands allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 12 further defines the electronic device of claim 1 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit. Claim 12 stands allowable for the same reasons set forth above in support of the allowance of claim 1.

Claim 13 further defines the electronic device of claim 1 wherein the scan storage circuit further comprises circuitry for causing each successive scan word **to be written from the scan storage circuit into the memory structure in parallel**, and for causing each successive scan word **to be read from the memory structure into the scan storage circuit in parallel**. Claim 13 stands allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Gorman specifically states the following:

> The shift register is utilized to collect the data that is received serially and then load multiple bits in parallel to the SRAM (because data is preferably written to the SRAM array in parallel operations and **not serially**)(paragraph [0007], lines 4-8).

Accordingly, Gorman fails to teach or suggest, "...circuitry for causing each successive scan word **to be written from the scan storage circuit into the memory structure in parallel**, and for causing each successive scan word **to be read from the memory structure into the scan storage circuit in parallel**", as further required by Claim 13.

Claim 14 further defines the electronic device of claim 1: "wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit" and "wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in parallel". Claim 14 stands allowable for the same reasons set forth above in support of the allowance of claim 1.

Claim 15 further defines the electronic device of claim 1: "wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells" and "wherein each set of N memory cells comprises N latches". Claim 15 stands allowable for the same reasons set forth above in support of the allowance of claim 1.

Claim 16 further defines the electronic device of claim 15 wherein each of the N latches comprises: "a first inverter having an input providing an input to the latch and an output providing an output of the latch" and "a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch". Claim 16 stands allowable for the same reasons set forth above in support of the allowance of claim 15.

Claim 17 further defines the electronic device of claim 1 wherein the memory structure, the scan storage circuit, and the control circuitry are all in a single integrated circuit. Claim 17 stands allowable for the same reasons set forth above in support of the allowance of claim 1.

Claim 19 further defines the method of claim 18 wherein the scan storage circuit is operable to receive a scan word consisting of N bits. Claim 19 stands allowable for the same reasons set forth above in support of the allowance of claim 18.

Claim 20 further defines the method of claim 19 and further comprising causing each successive scan word to be read from the scan storage circuit during a same time period as causing corresponding successive scan words to be written into the scan storage circuit. Claim 20 stands allowable for the same reasons set forth above in support of the allowance of claim 19.

Claim 21 further defines the method of claim 19 and further comprising causing each successive scan word to be serially read by shifting bits out from the scan storage circuit during a same time period as causing corresponding successive **scan words to be serially written** by shifting bits into the scan storage circuit. Claim 21 stands allowable for the same reasons set forth above in support of the allowance of claim 19. Moreover, Gorman specifically states the following:

> The shift register is utilized to collect the data that is received serially and then load multiple bits in parallel to the SRAM (because data is preferably written to the SRAM array in parallel operations and **not serially**)(paragraph [0007], lines 4-8).

Accordingly, Gorman fails to teach or suggest, "...further comprising causing each successive scan word to be serially read by shifting bits out from the scan storage circuit during a same time period as causing corresponding successive **scan words to be serially written** by shifting bits into the scan storage circuit", as further required by Claim 21.

Claim 22 further defines the method of claim 21: "wherein the step of causing successive scan words to be written from the scan storage circuit into the memory structure comprises **writing each successive scan word from the scan storage circuit into the memory structure in parallel**" and "wherein the step of causing successive scan words to be read from the memory structure into the scan storage circuit comprises **writing each successive scan word from the memory structure into the scan storage circuit in parallel**". Claim 21 stands allowable for the same reasons set forth above in support of the allowance of claim 19. Moreover, Gorman specifically states the following:

> The shift register is utilized to collect the data that is received serially and then load multiple bits in parallel to the SRAM (because data is preferably

written to the SRAM array in parallel operations and **not serially**)(paragraph [0007], lines 4-8).

Accordingly, Gorman fails to teach or suggest, "wherein the step of causing successive scan words to be written from the scan storage circuit into the memory structure comprises **writing each successive scan word from the scan storage circuit into the memory structure in parallel**" and "wherein the step of causing successive scan words to be read from the memory structure into the scan storage circuit comprises **writing each successive scan word from the memory structure into the scan storage circuit in parallel**", as further required by Claim 21.

2) Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gorman in view of Colon-Bonet, (US 6,970,897). Applicant respectfully traverses this rejection as set forth below.

Claim 10 further defines the electronic device of claim 9 wherein N is selected from a group consisting of 128, 64, 32, 16, 8, and 4. Even if, arguendo, Colon-Bonet teaches a system where the width of an electronic device is selected from a group consisting of 128, 64, 32, 16, 8, and 4, as suggested by Examiner, the reference fails to teach or suggest the previously described deficiencies of the Gorman reference. As such, any combination of Gorman and Colon-Bonet fails to teach all of the elements of Claim 10.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy

this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Similarly, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so.**" *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

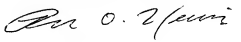
Similarly, although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. As discussed above, Examiner has failed to set forth any legitimate suggestion or motivation, either in the references themselves or in the knowledge generally available to one or ordinary skill in that art, to modify Gorman in view of Colon-Bonet, as suggested by Examiner. Second, there must be a reasonable expectation of success. Examiner has failed to provide any evidence that modifying Gorman in view of Colon-Bonet will result in an apparatus that would successfully implement all of the elements of Claim 10. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations (MPEP § 2143). Applicant respectfully submits that the Examiner has failed to establish all three criteria. Accordingly, Claim 10 is patentable under 35 U.S.C. § 103(a) over Gorman in view of Colon-Bonet.

Claims 1-22 stand allowable. Applicant respectfully requests withdrawal of the rejections and allowance of the application at the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicant

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418